REMARKS

Claims 1 and 13-15 are all the claims pending in the application.

Applicant thanks the Examiner for considering the references cited in the IDS filed on October 11, 2006.

Also, Applicant thanks the Examiner for acknowledging the drawings filed on December 12, 2006.

Applicant has Amended claim 1 to further clarify Applicant's claimed invention.

Also, with this Amendment, Applicant adds claim 15. Applicant submits that claim 15 is patentable at least by virtue of its respective dependency, as well as the features set forth therein.

Claim Objections

Claim 1 has been objected to for minor informalities. Claim 1 is amended to overcome this objection. Thus, withdrawal of this objection is respectfully requested.

Claim Rejections - 35 U.S.C. § 103

Claims 1, 13, and 14 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno (USP 6,218,878) in view of Reimann (USP 6,486,720). Applicant traverses these rejections because Reimann, either alone or in combination with Ueno, fails to disclose or suggest all of the claim limitations . Specifically, the references fails to disclose or suggest at least the following:

Claim 1:

wherein, since a size of the transistors constituting the first and second data-hold circuit is smaller than a size of the transistors constituting the first and second data reading circuit, in the working operation range, it causes a difference to the currents flowing through the first and second data-hold circuits and the currents flowing through the first and second data reading circuits, and thereby, the **currents flowing through the first and second data-hold circuits are lower than the currents flawing through the first and second data reading circuits**

Ueno and Reimann do not disclose that the size of the transistors constituting the data-hold circuit is smaller than the size of the transistors constituting the data reading circuit, and thereby, in the working operation range, the current that flows through the data-hold circuit is lower than the current that flows through the data reading circuit.

One characteristic of the claimed invention is that the operating speed of the flip-flop circuit makes a difference in the current that flows through the data-hold circuit and the current that flows through the data reading circuit.

Therefore, the size of transistors Q3, Q4 and Q6 (Q12, Q13 and Q15) constituting the data-hold circuit in Fig. 1 is smaller than the size of the transistors Q1, Q2 and Q5 (Q10, Q11 and Q14) constituting the data reading circuit.

However, since the current source of the data-hold circuit and the data reading circuit is common (q5 and q12 in fig. 16 of Ueno, and IQ in the fig. of Reimann), the current that flows

through the data-hold circuit and the current that flows through the data reading circuit is constant. Consequently, since the same current that flows through the data reading circuit flows through the data-hold circuit, large-current flows through the transistors (T5 and T6 in the fig. of Reimann) constituting the data-hold circuit. To avoid it, in JP-A-1993-48402 that is described in the specification of the present invention as conventional art and in Ueno (fig. 1), the current sources of the data-hold circuit and the data reading circuit are set apart (Q7 and Q16 in fig. 2 of the specification of the present invention), to connect the data-hold circuit side and the data reading circuit side respectively (page 4, line 16 to page 5, line 10; fig. 2).

One characteristic of the claimed invention is that the size of three transistors Q3, Q4 and Q6 (Q12, Q13 and Q15) constituting the data-hold circuit is smaller than the size of the three transistors Q1, Q2 and Q5 (Q10, Q11 and Q14) constituting the data reading circuit. Thus, without changing connection of the current source, the current that flows through the data-hold circuit is lower than the current that flows through the data reading circuit according to the operating speed of the flip-flop circuit.

Therefore, the claimed invention differs from the references because the size of transistor Q3 (Q15) constituting the data-hold circuit is smaller than the size of the transistor constituting the data reading circuit.

Further, Ueno does not disclose the relation between the size of transistors constituting the data-hold circuit and the size of the transistors constituting the data reading circuit.

Furthermore, Ueno does not disclose that the operating speed of the flip-flop circuit makes a difference on the current that flows through the data-hold circuit and the current that flows through the data reading circuit.

In Reimann, the current that flows through the data-hold circuit is **not** lower than the current that flows through the data reading circuit, and the same current flows through the data-hold circuit and the data reading circuit.

Additionally, Reimann does not disclose the relation between transistors TI and T2. In the configuration of Reimann, the current that flows through the data-hold circuit and the data reading circuit does not change according to the operating speed of the flip-flop circuit.

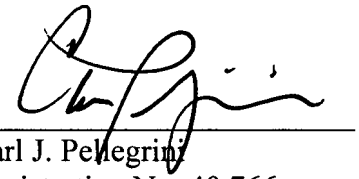
Therefore, at least for the above reasons, Applicant respectfully submits that claim 1 is patentable over the applied references and request the Examiner to withdraw the rejection.

Additionally, claims 13-15 should be allowable at least based on their dependency.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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